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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,415	01/15/2004	Hisashi Kaneko	04173.0441	3384

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FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
SHARON, AYAL I	
ART UNIT	PAPER NUMBER
2123	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/19/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,415	KANEKO ET AL.	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/15/04,8/12/04,11/10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-22 of U.S. Application 10/757,415 filed on 1/15/2004 are currently pending.
2. The application claims benefit of Japanese Application P2003-344526, filed on 10/2/2003.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.
5. Independent claim 1 recites the limitation of "forming the aggregate of simulation circuit patterns on a substrate", but the specification is silent as to how to form the aggregate of simulation circuit patterns on a substrate. All dependent claims inherit this defect.

6. Independent claim 8 recites the limitation of "forming the aggregate of the simulation circuit patterns on each of plural substrates", but the specification is silent as to how to form the aggregate of simulation circuit patterns on plural substrates. All dependent claims inherit this defect.
7. Independent claims 13 and 18 are directed to the substrate and substrate group, but the specification is silent as to how to form the aggregate of simulation circuit patterns on one or plural substrates. All dependent claims inherit this defect.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. The prior art used for these rejections is as follows:
    a. Muddu, S. et al. "Repeater and Interconnect Strategies for High-Performance Physical Designs." Proc. XI Brazilian Symposium on IC Design. Sept.30 – Oct.3, 1998. pp.226-231. (Hereinafter "**Muddu**").
10. **Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Muddu.**
11. In regards to Claim 1, Muddu teaches the following limitations:

> *1. A simulation circuit pattern evaluation method, comprising:*
> *designing an aggregate of simulation circuit patterns,*

(See Muddu, especially: "Abstract" and "Introduction". VLSI designs are aggregates of simulation circuit patterns. The Introduction expressly teaches a "7-layer" metal process.)

which simulate a circuit pattern of a semiconductor integrated circuit,

(See Muddu, especially: "Introduction", which teaches that "Table 1 reproduces several technology projections from the 1997 SIA National Technology Roadmap for Semiconductors ...the number of wiring layers is now projected to reach 9 layers ..."

See also "Interconnect Strategies", which expressly teaches that "This work provides studies of interconnect tuning, optimal number of repeaters, optimal repeater size, and critical repeater insertion length for various wiring layers.")

by combining plural geometrical structure defining parameters

(See Muddu, especially: The wire width and spacing parameters defined in Table 5, in "2.5. Effect of Interconnect Slew Time", and in "3. Effects of Shield Wiring. Examiner notes that the parameters in Table 1 of the instant application include "wiring formation width" and "wiring formation height")

respectively having at least two states

(See Muddu, especially: The wire width and spacing parameters defined in Table 5, in "2.5. Effect of Interconnect Slew Time", and in "3. Effects of Shield Wiring. Examiner notes that the "states" are defined in paragraph [0026] of the instant application as corresponding to two or three distinct values for the wiring formation parameters.)

in such a manner that the respective states appear the same number of times in the respective geometrical structure defining parameters;

(See Muddu, especially: The wire width and spacing parameters shown in Tables 3 to 6, and in "2.5. Effect of Interconnect Slew Time", and in "3. Effects of Shield Wiring.)

forming the aggregate of simulation circuit patterns on a substrate;

(See Muddu, especially: "2.4 Critical Repeater Insertion Length", Tables 3 and 4, and "Interconnect Strategies")

and evaluating the formed aggregate of the simulation circuit patterns.

(See Muddu, especially: "2.4 Critical Repeater Insertion Length", Tables 3 and 4, and "Interconnect Strategies")

12. In regards to Claim 2, Muddu teaches the following limitations:

2. The simulation circuit pattern evaluation method as set forth in claim 1,

wherein said forming includes forming the aggregate of the simulation circuit patterns on each of a plurality of the substrates with a process condition which is different for each of the substrates; and

wherein said evaluating includes separately evaluating the aggregate of the simulation circuit patterns on each of the substrates.

13. In regards to Claim 3, Muddu teaches the following limitations:

3. The simulation circuit pattern evaluation method as set forth in claim 1,

wherein said forming is performed with a predetermined process condition; and

wherein said evaluating includes evaluating a suitability of a circuit pattern of a semiconductor integrated circuit for the predetermined process condition based on the aggregate of the simulation circuit patterns.

14. In regards to Claim 4, Muddu teaches the following limitations:

4. The simulation circuit pattern evaluation method as set forth in claim 1,

wherein the geometrical structure defining parameters are parameters which define a geometrical structure of a wiring.

15. In regards to Claim 5, Muddu teaches the following limitations:

5. The simulation circuit pattern evaluation method as set forth in claim 4,

wherein the parameters which define the geometrical structure of the wiring include at least any one of a wiring formation width, a wiring formation length, a via hole formation position, a dummy wiring group formation position, a wiring group formation length and an existence of dummy via hole.

16. In regards to Claim 6, Muddu teaches the following limitations:

6. The simulation circuit pattern evaluation method as set forth in claim 1,

wherein the geometrical structure defining parameters are parameters which define a geometrical structure of a transistor.

17. In regards to Claim 7, Muddu teaches the following limitations:

7. The simulation circuit pattern evaluation method as set forth in claim 6,

wherein the parameters which define the geometrical structure of the transistor include at least any one of an active area dummy density, an active area dummy size, an active area dummy shape, a gate electrode formation width, a gate electrode formation length, a contact hole diameter, a degree of miss-alignment, and a shallow trench isolation formation width.

18. In regards to Claim 8, Muddu teaches the following limitations:

8. A manufacturing method of a semiconductor integrated circuit, comprising:

designing an aggregate of simulation circuit patterns,

(See Muddu, especially: "Abstract" and "Introduction". VLSI designs are aggregates of simulation circuit patterns. The Introduction expressly teaches a "7-layer" metal process.)

which simulate a circuit pattern of a semiconductor integrated circuit,

(See Muddu, especially: "Introduction", which teaches that "Table 1 reproduces several technology projections from the 1997 SIA National Technology Roadmap for Semiconductors ...the number of wiring layers is now projected to reach 9 layers ..."

See also "Interconnect Strategies", which expressly teaches that "This work provides studies of interconnect tuning, optimal number of repeaters,

optimal repeater size, and critical repeater insertion length for various wiring layers.")

by combining plural geometrical structure defining parameters

(See Muddu, especially: The wire width and spacing parameters defined in Table 5, in "2.5. Effect of Interconnect Slew Time", and in "3. Effects of Shield Wiring. Examiner notes that the parameters in Table 1 of the instant application include "wiring formation width" and "wiring formation height")

respectively having at least two states

(See Muddu, especially: The wire width and spacing parameters defined in Table 5, in "2.5. Effect of Interconnect Slew Time", and in "3. Effects of Shield Wiring. Examiner notes that the "states" are defined in paragraph [0026] of the instant application as corresponding to two or three distinct values for the wiring formation parameters.)

in such a manner that the respective states appear the same number of times in the respective geometrical structure defining parameters;

(See Muddu, especially: The wire width and spacing parameters shown in Tables 3 to 6, and in "2.5. Effect of Interconnect Slew Time", and in "3. Effects of Shield Wiring.)

forming the aggregate of the simulation circuit patterns on each of plural substrates with a process condition which is different for each of the substrate;

(See Muddu, especially: "2.4 Critical Repeater Insertion Length", Tables 3 and 4, and "Interconnect Strategies")

detecting a process condition which is suitable for the aggregate of the simulation circuit patterns by separately evaluating the formed aggregate of the simulation circuit patterns on each of the substrate; and

(See Muddu, especially: "2.4 Critical Repeater Insertion Length", Tables 3 and 4, and "Interconnect Strategies")

forming the circuit pattern with the detected process condition.

(See Muddu, especially: "2.4 Critical Repeater Insertion Length", Tables 3 and 4, and "Interconnect Strategies")

19. In regards to Claim 9, Muddu teaches the following limitations:

> *9. The manufacturing method of a semiconductor integrated circuit as set forth in claim 8,*
> *wherein the geometrical structure defining parameters are parameters which define a geometrical structure of a wiring.*

(See Muddu, especially: The wire width and spacing parameters defined in Table 5, in "2.5. Effect of Interconnect Slew Time", and in "3. Effects of Shield Wiring. Examiner notes that the parameters in Table 1 of the instant application include "wiring formation width" and "wiring formation height")

20. In regards to Claim 10, Muddu teaches the following limitations:

> *10. The manufacturing method of a semiconductor integrated circuit as set forth in claim 9,*
> *wherein the parameters which define the geometrical structure of the wiring include at least any one of a wiring formation width, a wiring formation length, a via hole formation position, a dummy wiring group formation position, a wiring group formation length and an existence of dummy via hole.*

(See Muddu, especially: The wire width and spacing parameters defined in Table 5, in "2.5. Effect of Interconnect Slew Time", and in "3. Effects of Shield Wiring. Examiner notes that the parameters in Table 1 of the instant application include "wiring formation width" and "wiring formation height")

21. In regards to Claim 11, Muddu teaches the following limitations:

> *11. The manufacturing method of a semiconductor integrated circuit as set forth in claim 8,*
> *wherein the geometrical structure defining parameters are parameters which define a geometrical structure of a transistor.*

(See Muddu, especially: "Introduction", which teaches that "Table 1 reproduces several technology projections from the 1997 SIA National Technology Roadmap for Semiconductors ...the number of wiring layers is now projected to reach 9 layers ..."

See also "Interconnect Strategies", which expressly teaches that "This work provides studies of interconnect tuning, optimal number of repeaters, optimal repeater size, and critical repeater insertion length for various wiring layers.")

22. In regards to Claim 12, Muddu teaches the following limitations:

> *12. The manufacturing method of a semiconductor integrated circuit as set forth in claim 11,*
> *wherein the parameters which define the geometrical structure of the transistor include at least any one of an active area dummy density, an active area dummy size, an active area dummy shape, a gate electrode formation width, a gate electrode formation length, a contact hole diameter, a degree of miss-alignment, and a shallow trench isolation formation width.*

(See Muddu, especially: The wire width and spacing parameters defined in Table 5, in "2.5. Effect of Interconnect Slew Time", and in "3. Effects of Shield Wiring. Examiner notes that the parameters in Table 1 of the instant application include "wiring formation width" and "wiring formation height")

23. **Claims 13-22 are rejected based on the same reasoning as claims 8-12. Claims 13-17 are apparatus ("substrate") claims, and claims 18-22 are apparatus ("substrate group") claims that recite limitations equivalent to those recited in method claims 8-12 and taught throughout Muddu.**

Conclusion

24. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

25. U.S. Patent Application 10/784,939, cited by the applicants in the IDS filed on 8/12/2004, has been published as U.S. PG-PUB 2004/0228186, and issued as U.S. Patent 6,975,953. This reference teaches the claimed subject matter (see

especially Fig.6 and associated text). The Japanese priority document of this reference, JP 2004-259894 A, was published too recently (9/16/2004) to qualify as prior art under 35 U.S.C. 102(a).

26. Oda, U.S. Patent 6,505,332. (Hereinafter "**Oda**"). Oda teaches the use of a "wire information file" in figures 5 and 6, and col.5, lines 49-63. This is similar to Table 1 and paragraph [0007] in the instant application. However, Oda does not expressly teach a fixed set of values, which the applicant calls "states" (see paragraph [0007] in the instant application). Instead, Oda teaches that the values are either constant (see col.2, line 58) or "a distributed constant value" (see col.2, lines 66-67).

27. Sakanushi, K. et al. "The Quarter-State-Sequence Floorplan Representation." IEEE Transactions on Circuits and Systems I. Mar. 2003. Vol.50, Issue 3, pp.376-386. (Hereinafter "**Sakanushi**"). Sakanushi defines "state" differently than in the instant application. Sakanushi defines "state" as "the configuration of one of [the] four corners" of a "room" in an integrated circuit floor plan. Sakanushi is therefore not relevant art.

28. Hung, W.-L. et al. "Interconnect and Thermal-aware Floorplanning for 3D microprocessors." 7th Int'l Symposium on Quality Electronic Design (ISQED '06). Mar.27-29, 2006. (Provides background information. Does not expressly teach a fixed set of values, which the applicant calls "states" (see paragraph [0007] in the instant application).

29. Sarrafzadeh, M. et al. "Single-layer Global Routing." IEEE Transactions on CAD of IC Circuits and Systems. Jan.1994. Vol.13, Issue 1, pp.38-47. (Provides background information. Does not expressly teach a fixed set of values, which the applicant calls "states" (see paragraph [0007] in the instant application).

30. Venkatesan, R. et al. "Optimal n-tier Multilevel Interconnect Architectures for Gigascale Integration (GSI)." IEEE Transactions on VLSI Systems. Dec. 2001. Vol.9, Issue 6, pp.899-912. (Provides background information. Does not expressly teach a fixed set of values, which the applicant calls "states" (see paragraph [0007] in the instant application).

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a bi-week, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753.

Any response to this office action should be faxed to (571) 273-8300, or mailed to:

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Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon
Art Unit 2123
December 1, 2006

ZOILA CABRERA
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100
12/8/06